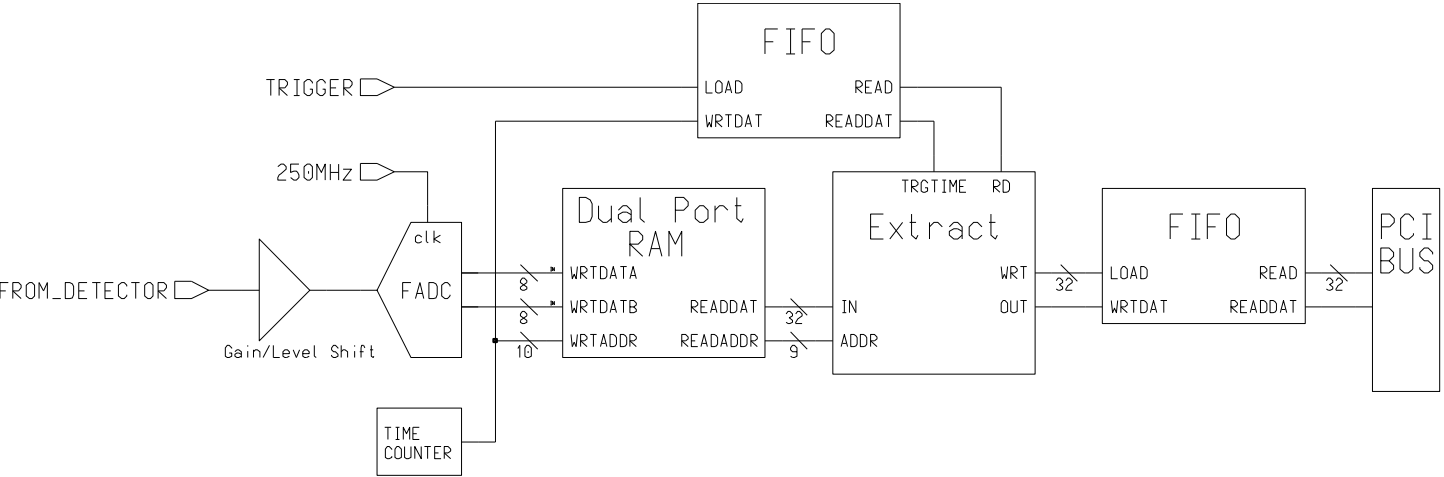
FIFO
TRIGGER
LOAD
READ
WRTDAT
READDAT
250MHz
clk
FROM_DETECTOR
FADC
Gain/Level Shift
Dual Port
RAM
WRTDATA
WRTDATB
WRTADDR
READDAT
READADDR
8
8
10
32
9
TRGTIME
RD
Extract
IN
ADDR
WRT
OUT
32
FIFO
LOAD
READ
WRTDAT
READDAT
32
PCI
BUS
TIME
COUNTER