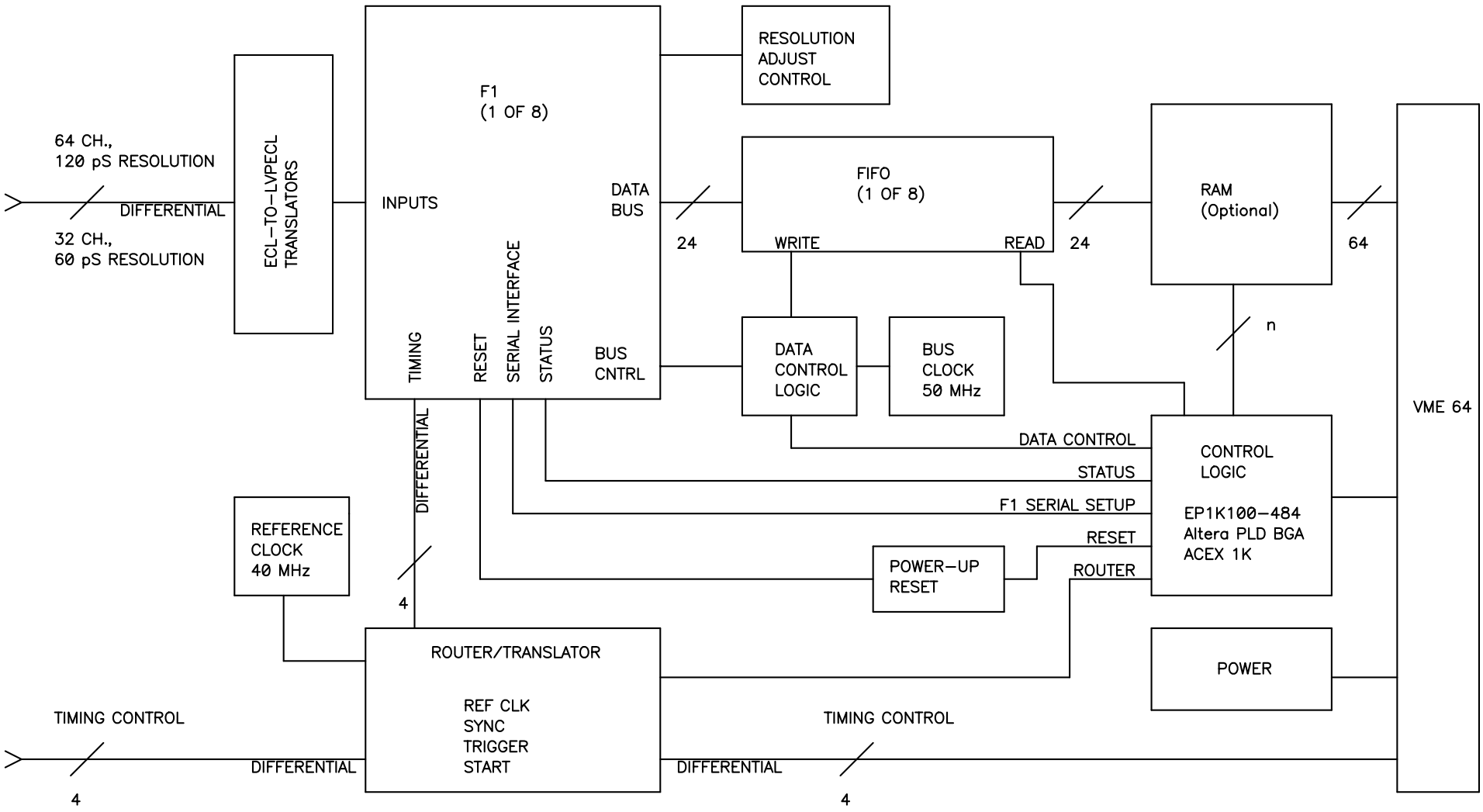
64 CH.,
120 pS RESOLUTION
DIFFERENTIAL
32 CH.,
60 pS RESOLUTION
ECL–TO–LVPECL
TRANSLATORS
F1
(1 OF 8)
INPUTS
DATA
BUS
TIMING
RESET
SERIAL INTERFACE
STATUS
BUS
CNTRL
RESOLUTION
ADJUST
CONTROL
24
FIFO
(1 OF 8)
WRITE
READ
24
RAM
(Optional)
64
n
DATA
CONTROL
LOGIC
BUS
CLOCK
50 MHz
VME 64
DATA CONTROL
STATUS
F1 SERIAL SETUP
RESET
ROUTER
CONTROL
LOGIC
EP1K100–484
Altera PLD BGA
ACEX 1K
DIFFERENTIAL
REFERENCE
CLOCK
40 MHz
4
POWER–UP
RESET
ROUTER/TRANSLATOR
REF CLK
SYNC
TRIGGER
START
POWER
TIMING CONTROL
DIFFERENTIAL
4
TIMING CONTROL
DIFFERENTIAL
4