

# HALL C RASTER VETO/FLAG GENERATOR

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## Abstract

When one rasters a beam over a target using a standard sign wave control signal, one finds that the beam tends to remain at the edges and corners of the target longer than in the center. This is due to the beam slowing down before reversing direction as it rasters back and forth. The extra time spent at the edges tends to cause anomalous results during certain nuclear physics experiments. This circuit tracks the X and Y raster waveforms and sends out a NIM and TTL veto/flag pulse when  $X^2 + Y^2$  is greater than a user set threshold based on the percent of the peak voltage on the Y input. This can be used to limit one's data to a circular region in the center of the target. This circuit automatically compensates for changing frequency and voltage to maintain a constant percent trigger from .4 V to 5 V peak to peak. Delay through the circuit is less than 30 nsec.

## Circuit Description and Results

The block diagram is shown in figure 1 and the circuit diagram is shown in figure 2. Both the X and Y inputs are squared using a precision analog multiplier. The squared waveforms are then added together and passed onto the comparator. The original Y input is also used to sense the peak amplitude of the driving waveform giving a DC voltage of the same value as the peak voltage. A user set percent of this peak amplitude (T) is then also squared using an analog multiplier and sent to the comparator. This triggers the comparator whenever

$$X^2 + Y^2 > T^2.$$

This VETO/FLAG output is easily seen to result any time X and Y are outside a circle of radius T.

On the circuit diagram one can see the heart of the circuit is the precision analog multiplier MPY634 from Burr-Brown[1] or, similarly, the AD534 from Analog

Devices[2]. These chips run on +/- 15V and the input voltage range is +/- 12V. The output voltage swing is +/- 12V with an offset of about +/- 50 mV. The bandwidth of the chip is 10MHz, however, the slew rate is only 20V/ $\mu$ s. The basic transfer function of the chip is

$$\text{Output} = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} + Z_2.$$

In this case we set  $X_2$ ,  $Y_2$  and  $Z_2$  to zero and put the same signal in both  $X_1$  and  $Y_1$ . Tuning the dynamic range, using a multiplier chip, can be a problem. The expected dynamic range of the driver waveforms is .4 V to 5 V peak-peak. If we put this into the multiplier directly we would have an output of 4 mV to .625V. Note that the squaring of the signal takes the negative portion of the peak and makes it positive. Thus the equation becomes

$$\text{Output} = \frac{1}{10} \left( \frac{V_{\text{pk-pk}}}{2} \right)^2 = \frac{V_{\text{pk-pk}}^2}{40}$$

Four mV is down in the noise of the circuit and the VETO/FLAG becomes quite unstable. There are three ways to adjust the dynamic range. The first is by just amplifying the input signal to reach the maximum output of the chip (12V for an input of 21.9V pk-pk). This gives us an output of 77 mV to 12V.

The second way to adjust the dynamic range involves the scale factor (SF) built into the chip. Instead of dividing by a SF of 10V, you can chose a smaller divisor. When you use this method, the input voltage is limited to a maximum of  $1.25 * \text{SF}$  and the smallest SF is 3V. If we used the smallest SF, we would get an output of 20.8 mV to 2.08V. If we also amplified the input waveform to the maximum input voltage of 7.5 pk-pk, we would get an output of 30 mV to 4.69 V.

The third way to adjust the dynamic range is to use an attenuator feedback connection suggested by the manufacturer to obtain a SF of unity. If we amplified the input to reach the maximum output of the chip, we again obtain an output of 77 mV to 12V as in the first method described above. Unfortunately, this method is accompanied with a reduction in bandwidth and an increase in offset voltage. Thus the first method of adjusting the dynamic range was chosen to obtain the best signal to noise at

the lowest voltage while staying within the dynamic range of the chip.

A very important chip is the comparator. The majority of fast comparators (< 80 nsec response time) run on 5V and thus can not be used with 12V input signals. Only one fast comparator was found to run on a 15V supply. The Elantec[3] EL2252CN has a 7 nsec response time with a TTL output.

The peak sensing circuit is basically out of an electronics cookbook, however, the input Y signal is offset by a positive voltage (an inverted summing with a negative voltage). This allows us to operate down to the .4V pk-pk input since the peak detection circuit usually needs at least 1V peak input to operate due to the break down resistance of the diode. The peak sensing circuit charges up to the peak of the input waveform and holds that voltage value with a slow decay. Another OP AMP is then used to subtract the same offset voltage added to the original signal. A potentiometer is used in the feedback loop of the threshold adjust OP

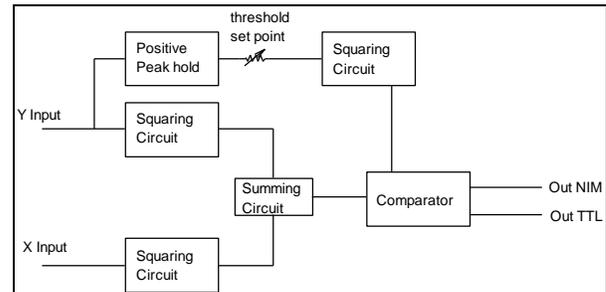


Figure 1: VETO/FLAG circuit block diagram.



original signal and of the signal with the TTL cut.

Figure 3 shows a horizontal slice through the center of the original X-Y input and a slice through center of the X-Y input with the TTL cut on the data for a 2.5 V peak to peak input waveform. The input data ranges from 340 to 864 while the cut data ranges from 390 to 812 or 9.5% to 90.0%. Figure 4 shows the original X-Y plot and the X-Y plot with the VETO/FLAG cut. With a .4 V peak to peak input the measured cutoffs were 11.4% and 88.6%. At a 5 V peak to peak input waveform the measured cutoffs were 9.4% to 90.0%.

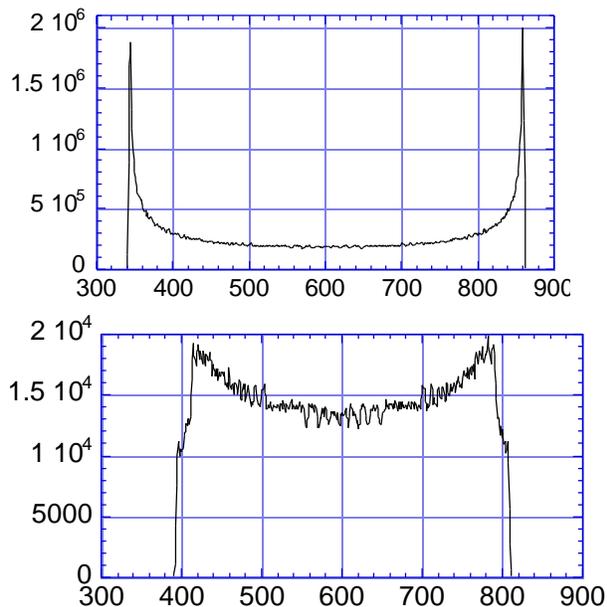


Figure 3: Top shows a slice through the original input X-Y plot at 2.5V pk-pk. bottom shows a cut through the X-Y plot with a VETO/FLAG TTL cut.

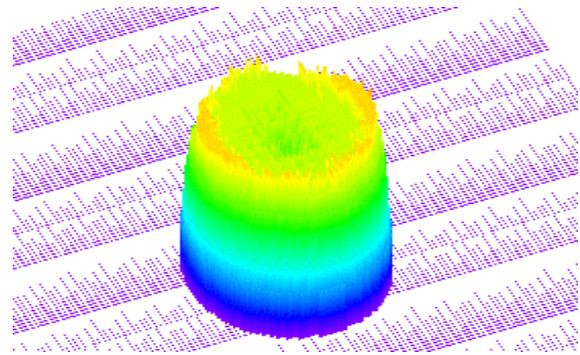
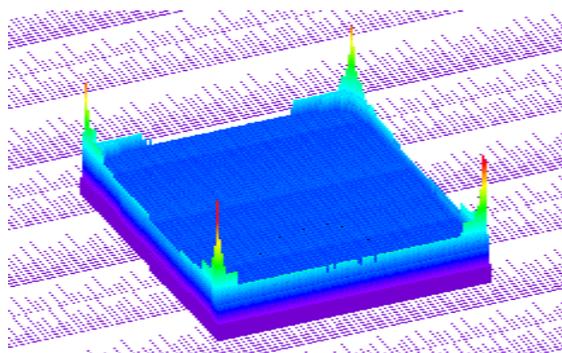
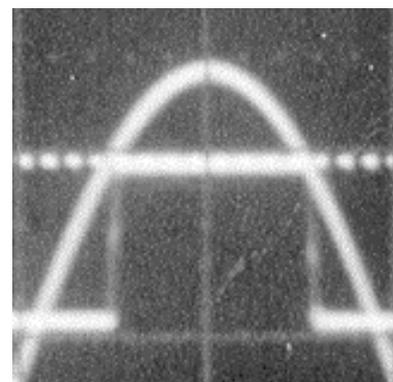
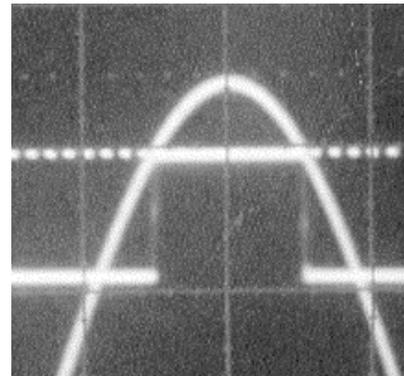


Figure 4: X-Y plots of the input raster pattern at 2.5V pk-pk. Top is the original pattern right is with the VETO/FLAG.

It was found that the speed of the multiplier played a roll in the output timing of the VETO/FLAG especially at with a 5 V pk-pk input. Since we are doubling the frequency by squaring the input signal (negative becomes positive), after about 40 kHz, a time delay in the VETO/FLAG pulse is apparent (fig. 5).



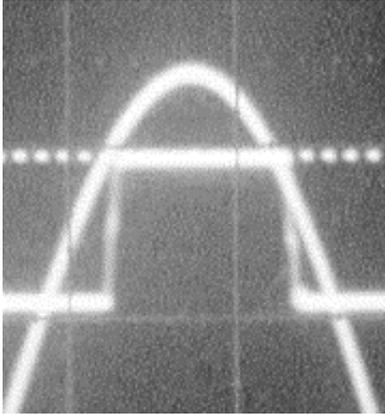


Figure 5: Delay of TTL pulse. Top, signal frequency is 20kHz, time scale is 10 $\mu$ s/div. Middle, signal frequency is 40kHz, time scale is 5 $\mu$ s/div. Bottom, signal frequency is 80kHz, time scale is 2.6 $\mu$ s/div.

#### REFERENCES

- [1] Analog Devices, Norwood, MA 02062.
- [2] Burr-Brown Corporation, Tucson, AZ 85734
- [3] Elantec Semiconductor Inc., Milpitas, CA 95035.
- [4] Wavetek, Research Triangle Park, NC 27709,
- [5] Phillips Scientific, Mahwah, NJ 07430.
- [6] National Instruments, Austin, TX 78730.
- [7] Sparrow Corporation, Mississippi State, MS 39762.